RT9430 Evaluation Board

Purpose

The RT9430 secure authenticator uses challenge and response authentication based on SHA-256 (FIPS 180-3) hash algorithm to ensure that the device is certified by the original manufacturer.

The purpose of the RT9430WTC evaluation board is to provide a hardware environment for engineer developing firmware. This document is intended to describe information of hardware and does not necessarily explain in detail the operation of the RT9430. Please read the RT9430 datasheet and application note for more detail information.

Table of Contents

Introduction

General Product Information

The RT9430 battery authenticator uses challenge and response authentication based on SHA-256 (FIPS 180-3) hash algorithm to ensure that the battery pack is certified by the original manufacturer. The device supports 34 bytes of programmable nonvolatile memory for users to access battery information, 4 bytes Device_ID for chip supplier information and system user information, and 8 bytes unique ROM ID for chip identification code. The RT9430 communicates over the single-wire interface.

The evaluation board was developed to bring out all of RT9430 pins. The evaluation board includes the RT9430 and passive components to quickly develop firmware in the system. The detail schematic, hardware and procedure will be described in the following section. The evaluation board dimension is 33mm x 2.65mm.

Product Feature

- **SHA-256 FIPS 180-3 Symmetric-Key-Based Secure Authentication Model**
- **34 Bytes of User NVM**
- **32 Bytes of Secret**
- **8 Bytes of ROM_ID**
- **4 Bytes of Device_ID**
- **Support NVM Write and Read Protect**
- **Supports Anonymous Authentication Mode**
- **Single-Wire Interface Bit Rate 50kbps, Supports**
- **Normal Mode and Fast Mode**
- **TWL-CSP 1.46x1.16mm (BSC) Package**

Key Performance Summary Table

Key Features	Evaluation Board Number : RT9430_PCM_C1-46X1-16_6L_V1
Input Voltage Range	2.8V to 5.0V
I/O Supply Voltage	1.8V
SHA256 Computation Current	1mA
SHA256 Computation Time	100µs
Default Marking & Package Type	RT9430WTC, TWL-CSP-6B 1.46x1.16 (BSC)

Bench Test Setup Conditions

Headers Description and Placement

Carefully inspect all the components used in the EVB according to the following Bill of Materials table, and then make sure all the components are undamaged and correctly installed. If there is any missing or damaged component, which may occur during transportation, please contact our distributors or e-mail us at evb_service@richtek.com.

Test Points

The EVB is provided with the connecter interfaces and pin names listed in the table below.

| Test Point	Pin Name	Comment (expected waveforms or voltage levels on test points)
P-	GND	Ground.
SWI	SWI	Single-wire interface. Support 1.8V I/O voltage.
P+	VDD	Power input. Support 2.8V to 5V input voltage.

Measurement Procedure

Please follow these simple steps to start developing your module.

1. Connect wire to P- and GND

2. Connect wire to P+ and VDD (2.8V to 5V)

3. Connect wire to SWI and GPIO (1.8V IO drive)

4. Refer to FW Sample Code (RT9430_SWI_source_code_V1_20190906.zip) for developing firmware in the system.
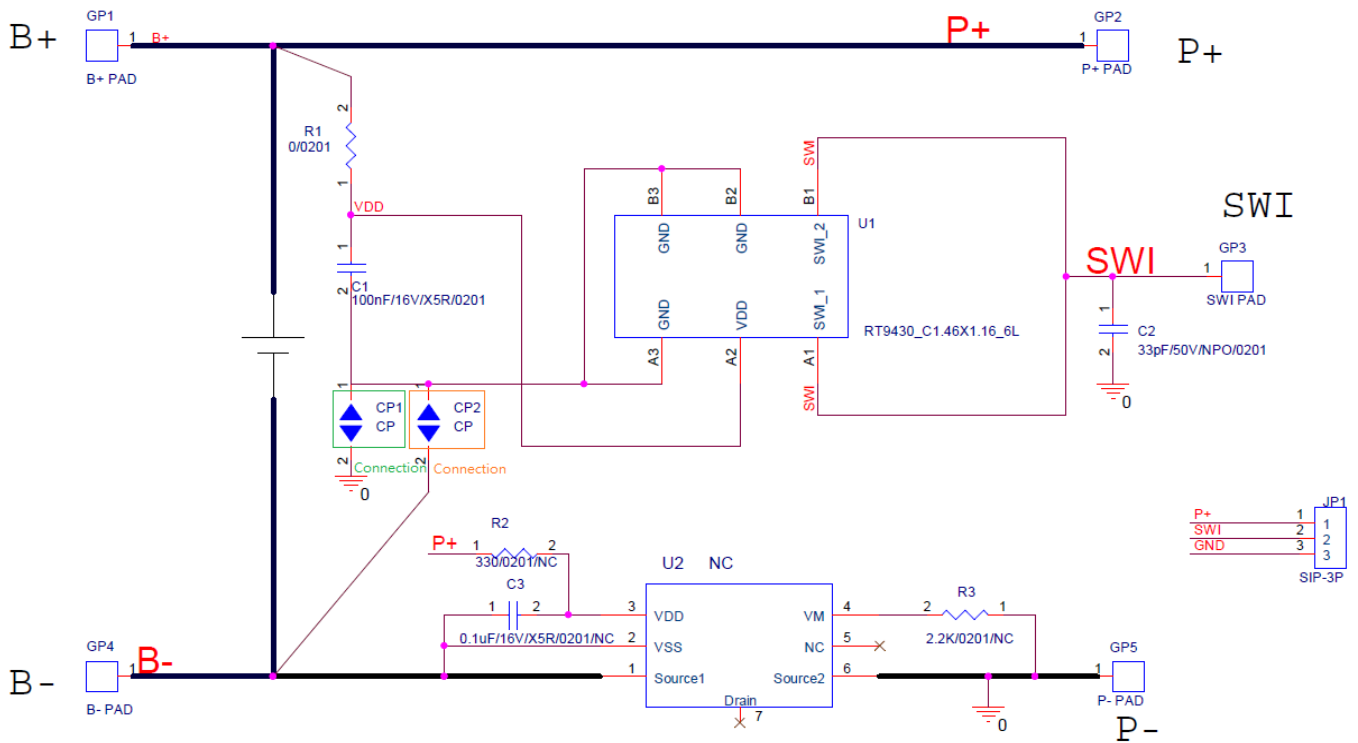
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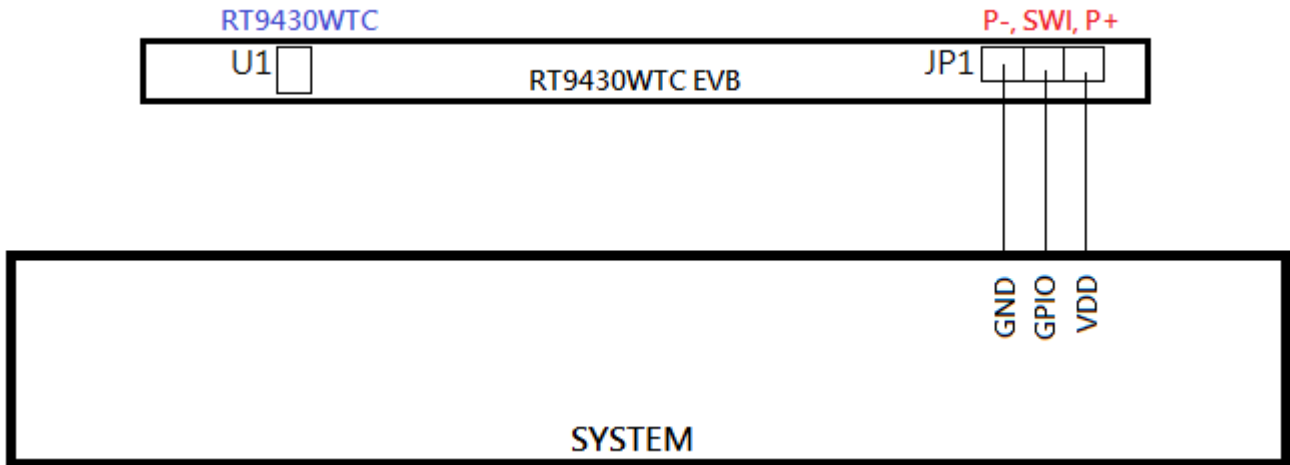
Typical Applicatin Circuit
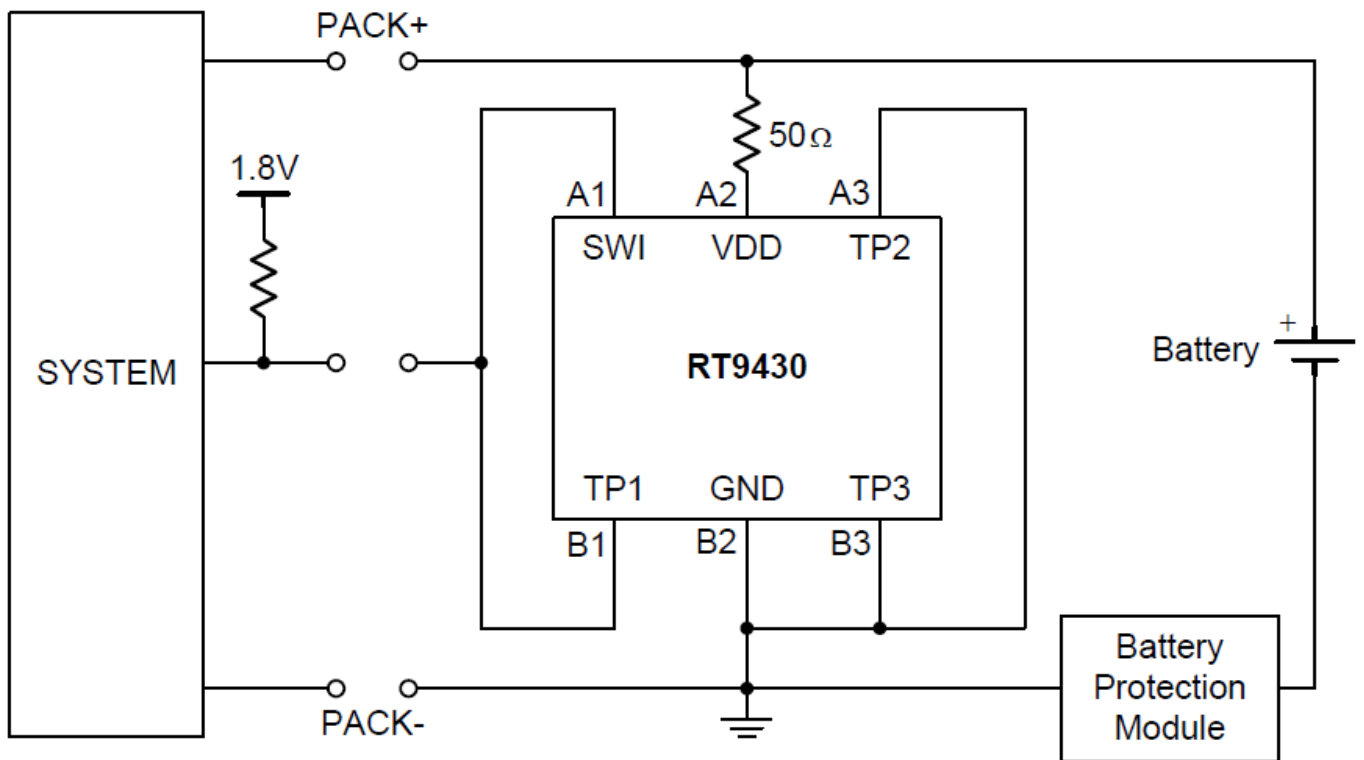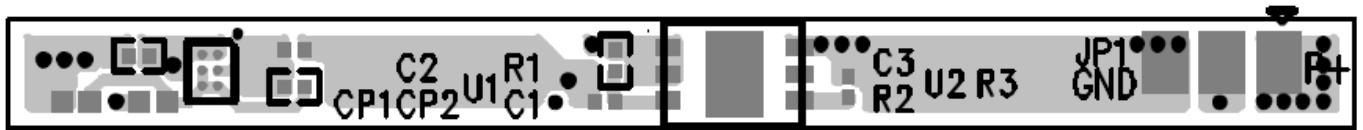
Schematic, Bill of Materials & Board Layout

EVB Schematic Diagram

Bill of Materials

Reference	Qty	Part Number	Description	Package	Manufacturer
U1	1	RT9430WTC	Authentication IC	TWL-CSP-6B 1.46x1.16 (BSC)	Richtek
R1	1	WR02X000 PAL	0R	R-0201	WALSIN
C1	1	0201X104K160CT	100nF/16V/X5R	C-0201	WALSIN
C2	1	0201N330J500CT	33pF/50V/NPO	C-0201	WALSIN

PCB Layout

Top View (1st layer)

PCB Layout—Inner Side (2nd Layer)

PCB Layout—Inner Side (3rd Layer)

Bottom View (4th Layer)

More Information

For more information, please find the related datasheet or application notes from Richtek website http://www.richtek.com.

Important Notice for Richtek Evaluation Board

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